Automotive Functional Safety

Adam Sherer
Product Management Group Director
Autonomous Cars Event
Detroit, MI
August 2015
Agenda

- ADASoC transforms electronics
- ISO 26262 and semiconductor verification
- Refining our verification processes
- But wait, there’s more
- Cadence in automotive electronics
- Call to action
Transformation of Transportation

**Connected Passenger**
- Seamless connectivity
- Security
- Bring your own device
- Personalized connected infotainment
- Voice & gesture control

**Intelligent Vehicle**
- Advanced driver assist systems
- Real-time car information & alerts
- Adaptive & predictive car safety

**Smart Transportation**
- Car-to-car
- Car-to-cloud
- Car-to-infrastructure
- Smart infrastructure
- Smart services
- Smart energy mgmt

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Infotainment  Autonomous Driving  Car-to-X
Automotive Electronics Trends

• Higher performance
  – Compute power: 2012 → 2016, 5X increase (20,000 DMIPS)
  – Network bandwidth: 1Mb → 100Mb → 1Gb

• Higher volume
  – 6000-8000 semiconductors per car (e.g. VW ships 10Mio cars)
  – Leveraging new automotive process technologies
    – GF40LP, 28nm FDSOI, T28nm,…
    – AEC-Q100 qualified

• Higher integration
  – Integration point will move from ECU to SiP/SoC
  – OEMs are starting with IC and board design
  – Better differentiation and IP protection
  – Less weight, less power, smaller form factor…
  – Is the tier1 supplier prepared for this technology shift?
ADAS + SoC = ADASoC transforms electronics

<table>
<thead>
<tr>
<th>Change</th>
<th>Implication</th>
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</thead>
<tbody>
<tr>
<td>Electronics differentiate OEMs</td>
<td>New competitors flood design chain</td>
</tr>
<tr>
<td>Higher IC counts</td>
<td>Power limitations of mobile platform</td>
</tr>
<tr>
<td>Functional safety</td>
<td>Labor intensive engineering expense</td>
</tr>
<tr>
<td>Multiple engine types</td>
<td>New IC families</td>
</tr>
<tr>
<td>Connected platform</td>
<td>Security</td>
</tr>
<tr>
<td>Massive processing</td>
<td>Smaller geometry</td>
</tr>
<tr>
<td>Quality above all else</td>
<td>Rigorous methodology</td>
</tr>
</tbody>
</table>
Cadence provides semiconductor scalability

- 25+ years in auto supply chain

- Comprehensive suite of tools, IP, and services for ECUs and semiconductors

- Focus on first pass success and end product quality
Agenda

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• ISO 26262 and semiconductor verification
  • Refining our verification processes
  • But wait, there’s more
  • Cadence in automotive electronics

• Call to action
Overview of ISO 26262 for Semiconductors

- ISO26262 is based upon a V-Model as reference process for the different phases of product development

- Requirements are predominately qualitative with a smaller quantitative component
  - All elements are data-driven

- As complexity grows quantitative will increase
Qualitative: Management of Functional Safety
Part 2, Clause 6

• General Safety Management (6.1, 6.2 and 6.3)
  – Assumes that the company has a defined, implemented and active
    Quality Management (QM) system
    – Organization-specific rules and processes for functional safety
    – Evidence of competence
    – Evidence of quality management
  – Imply Safety Culture, Communication, Qualification of Employees

• Design Development and Safety Management (6.4)
  – Require Project Manager and Safety Manager
    – A project manager shall be appointed at the initiation of the item development
    – The project manager shall be given the responsibility and the authority to ensure:
      – the safety activities required to achieve functional safety are performed
      – compliance with ISO 26262 is achieved
    – The project manager shall ensure that the safety manager is appointed
    – The role of the safety manager can be fulfilled by the project manager
      – The safety manager shall be responsible for the planning and coordination of the functional safety activities
        in the development phases of the safety lifecycle
Qualitative: Product Development in Hardware
Part 5, Clauses 5,6,7,8

• Clause 5 define the product development at the HW level
  – Project plan and Safety plan are being actualized and extended

• Clause 6 define the specification of HW Safety requirements
  – Safety mechanism to detect, tolerate or to flag internal and external errors
  – Include HW metrics
    – Single point faults metric (SPFM): system architecture can detect single fault
    – Latent faults metric (LFM): the system architecture is suitable to detect multiple faults

• Clause 7 define HW design and verification in accordance with specification and the safety requirements
  – Blocks: Sensors, CPU, Actuators, etc.
  – Components: Resistors, Capacitors, Transistor, etc.
  – Modules: Power Supply, Memory, etc.
  – Safety traceability is at module level and inherits the higher ASIL classification
Quantitative: Hardware Fault Classification

• Part 5, Clause 8 classify the HW faults
  – $\lambda_{SPF}$, Single Point Fault. Non tolerated fault violating Safety requirements
  – $\lambda_{RF}$, Residual Faults. Faults not detected by any mechanism and lead to a violation of Safety requirements
  – $\lambda_{MPF}$, Multiple Point Fault. Combination of independent faults which may lead to a violation of Safety requirements
    – Perceived (P), Detected (D) or Latent (L)
  – $\lambda_{S}$, Safe Faults. Do not effect the Safety requirements

• These faults contribute to calculate the failure rate $\lambda$
  $$\lambda = \lambda_{SPF} + \lambda_{RF} + \lambda_{MPF} + \lambda_{S}$$

FIT = Failures In Time
1 failure in $10^9$ device hours

<table>
<thead>
<tr>
<th>ASIL</th>
<th>Failure Rate</th>
<th>FIT</th>
<th>Severity</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>&lt;10^{-8}/hour</td>
<td>&lt; 10</td>
<td>Required</td>
</tr>
<tr>
<td>C</td>
<td>&lt;10^{-7}/hour</td>
<td>&lt; 100</td>
<td>Required</td>
</tr>
<tr>
<td>B</td>
<td>&lt;10^{-7}/hour</td>
<td>&lt; 1000</td>
<td>Advised</td>
</tr>
<tr>
<td>A</td>
<td>&lt;10^{-6}/hour</td>
<td>&lt; 1000</td>
<td>Informative</td>
</tr>
</tbody>
</table>
Hardware Fault Classification

Non Safety related fault
- Non dangerous fault

Safety related fault
- Detected and Perceived multiple fault
- Latent multiple fault
- Residual and Single point fault

No violation of Safety Goals

Maximize detection of multi-point latent faults
Maximize detection of single point faults

Failure Rate $\lambda$

$\lambda_S$  $\lambda_{MPF,DP}$  $\lambda_{MPF,L}$  $\lambda_{RF} + \lambda_{SPF}$
Hardware Fault Classification

• Maximize detection of **single point faults**
  – Detected and handled by system within system safety response time

• Maximize detection of **multi-point latent faults**
  – Detected and handled within hours through test algorithms

<table>
<thead>
<tr>
<th>Metrics</th>
<th>ASIL A</th>
<th>ASIL B</th>
<th>ASIL C</th>
<th>ASIL D</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPFM</td>
<td>Not relevant</td>
<td>(\geq 90%)</td>
<td>(\geq 97%)</td>
<td>(\geq 99%)</td>
</tr>
<tr>
<td>LFM</td>
<td>Not relevant</td>
<td>(\geq 60%)</td>
<td>(\geq 80%)</td>
<td>(\geq 90%)</td>
</tr>
</tbody>
</table>
Timing Aspect Consideration in ISO 26262

- As shown in Part 1, Figure 4 the system must be able to detect faults and transition to safe state within a specific time (FTTI) otherwise the fault can become a system level hazard.
- To impact SPFM, any diagnostics must execute within the FTTI.
- To impact LPFM, any diagnostics must execute once per drive cycle.

- Fault Reaction Time: time-span from the detection of a fault to reaching the safe state.
- Diagnostic Test Interval: amount of time between the executions of online diagnostic tests by a safety mechanism.
ISO 26262 and SOC development

• ISO 26262 does not impose any specific diagnostics to be implemented

• Some recommendation are listed in Part 5, Table D.6 for some basic design elements
  – Memory BIST, Parity, EDC, CRC, Redundancy, etc

• The IC developer must demonstrate the performance of implemented diagnostics
  – Typically this is done with fault injection

• Fault injection techniques can be used to establish the ratio of safe vs. dangerous faults

EDC = Error Detection and Correction
CRC = Cyclic Redundancy Check
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ISO 26262 standard documents functional safety
Builds on dependability that starts with functional verification

1. Safety culture
   ─ Requirements tracing from system to component
   ─ Prevents problems from arising

2. Quality measurement
   ─ Functional verification at all levels of abstraction and for all system elements
   ─ Safety verification measures response of systems to undesired/unplanned events

3. Documentation
   ─ Document tool confidence level (TCL) to show that tools did not inject or fail to detect safety violations
   ─ Document complete compliance (safety manual) per product (semi or ECU)
Safety verification has been labor intensive

Rewriting verification environment to fit traditional tool flow

Safety engineer research

Custom scripts to extract safety data

SDS = Cadence® System Development Suite™
ADE = Cadence Virtuoso® Analog Design Environment

Observation and manual documentation

Excel spreadsheets

ISO 26262

Safety Manual

Requirements

Functional Verification

Safety Verification

TCL
Verification Measures System Dependability

• Directed test - specific sequence of signal input
  – Best for connectivity verification and corner cases
  – Typically Verilog/VHDL behavioral, C/C++, data files
• Assertion based – properties verify behavior
  – Best for automating design checks and protocol verification
  – Typically SystemVerilog but also PSL and OVL (Verilog) code
• Constrained random – coverage driven verification
  – Best for comprehensive IP verification including configurations
  – Requires object oriented programming knowledge
  – Typically SystemVerilog or e code using a base class library (UVM)
• Mixed-signal – analog and digital using methods above
  – Transistor models only support connectivity and limited functionality
  – Verilog/VHDL AMS models support functional verification
  – Digital Mixed Signal (SystemVerilog) supports coverage driven
What is Metric Driven Verification (MDV)

- A codified verification methodology utilizing metrics, versus estimates, to define release criteria and thus verification signoff

- Key Enablers of MDV for Silicon & Systems Suppliers
  - Empowers management with clear visibility to progress, gaps, owners and issues
  - Is proven and scalable verification process, an industry standard
  - Drives quality improvements, as ‘you can only improve what you can clearly measure’
  - Returns greater productivity and resource utilization
Example FPGA/ASIC Verification Process

Flow Diagram

- **Objects:**
  - Logical
  - Command
  - Data
  - Processes
  - Tools
  - Objects

- **Data:**
  - Analog & Digital
  - Requirements

- **Enterprise System**
  - Specification
  - Verification Planning

- **Analog Capture / Layout**
  - Schematic Design
  - Simulation

- **Virtuoso DFII**
  - Model Creation
  - SMG
  - amsDmv
  - vManager
  - vPlan

- **In-house + 3rd party IP**
  - Testbench & Design Creation

- **Digital & Analog Sim**
  - Incisive
  - Simulation
  - MS Sim

Source: CDNLive Sept 2014

Analog Behavioral Model Creation
Direct verification shifts to MDV to scale

**With MDV**
- 1M Gate Design
- 10 Key Features
- 10 Sub-Functions Per Feature
- 100 Functional Plan Elements

**Functional Closure Possible**
- Functional Coverage
- Use Case Coverage
- Plan Coverage
- Specification Coverage
- Structural Coverage

**Functional Closure Impossible**
- ...But Structural Closure Is Possible
- RTL Code Coverage
- Toggle Coverage
- FSM Coverage
- Expression Coverage

1M Gate Design
30,000 Lines of Verilog Code
2000 Register Bits
$2^{2000}$ Verification States
Safety verification programs need to shift as well

- **Brute force** – all fault types on all faults’ insertion points
  - Becomes computationally impossible after $10^6$ gates
- **Constrained random** – sampling within safety-critical area
  - Combines randomized fault injection with coverage analysis
- **Formal guided** – reduce fault list without simulation
  - Operates on subset of overall design and does not support analog
Functional Safety Verification Flow Requirements

• Automate fault simulation execution
  – Eliminate testbench refactoring

• Safety requirements tracing
  – Integrate regression throughout for compliance metrics
  – Integrate permanent and transient fault simulation

• High performance/capacity
  – Gate-level, Verilog, and VHDL
  – Digital / mixed-signal simulation
  – Verify with IEEE languages
Safety and Function Verification are One Flow

- **Verify correct system behavior**
  - Use metrics to trace completeness of digital and analog verification
  - Tests include both positive and negative testing

- **Verify correct system response**
  - Use metrics to trace fault injection to safety system output
  - Tests enough fault injection to achieve confidence in safety systems
Safety analysis for ISO26262 IDs single point(s) of failure (SPF)

• Module
  – Contains basic functionality
  – May contain part of the safety mechanism e.g. fault tolerant functionality

• Functional output (F-O)
  – Interface to other modules
  – Safety violation at F-O is propagated to system
  – May contain many pins (> 1k)

• Checker
  – Contains part of the safety mechanism (checks if the output is valid)

• Checker output (C-O)
  – Signals the detection of a fault
  – Normally contains only a few lines (safety alarms)
Functional safety verification results

Multiple fault types for 26262
- Single event upset (SEU)
- Stuck at 0 or 1 (SA0/SA1)
- Single event transient (SET)

Simulates unaltered DUT
- Fault identification during elaboration
- Faults injected during simulation
- Support Verilog/VHDL for gates/RTL
- Faults can propagate through mixed-signal, low-power, assertions, etc.

Automates safety verification
- Efficiently executed fault simulations in modern regression environments
- Highlights potentially detected and undetected faults runs for further debug

Verification environment reuse
- Supports SystemVerilog/UVM, SystemC, e
Automotive functional safety verification

• Dependability and safety are system requirements
  – ADAS driving demand across OEMs, Tier1s, and Semis
  – Growing interest for industrial, medical, and aero & defense

• Expanding functional safety solution
  – Fault injection simulation
  – Requirements tracing for faster ISO26262 convergence
  – Broadening solution beyond RTL and gates

• Partnering for successful deployment
  – Consultative engagements, with 3rd party collaboration option
  – Adoption of existing technology and previews of upcoming ones
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System Level Design Fault Considerations

• Defined by untimed transaction-based design
  – Targeted to hardware/software co-design
  – May include algorithmic models for analog

• Enables early analysis of safety systems
  – Analyze failure reporting response time
  – Identify safety-critical systems

• Challenges: new fault models
  – Abstract data types do not have simple bit-faults
  – Ex. enum – how do you fault “orange”?  
  – Ex. struct – Do you fault individual data fields?
Functional Safety and DFT are Related

• Safety is not a whole subset of DFT
  – Transient faults typically are not part of manufacturing-oriented DFT

• Safety implementation sometimes supplanted by BIST
  – LBIST and MBSIT provide in-device safety checks
  – Cost is area and performance

• ATPG methods generate more faults than safety needs
  – Comprehensive nature can fault all device inputs
  – ATPG engines are fast for stuck-at faults

• Bottom-line – both safety and DFT are required
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System Design Enablement for Automotive
From chip to end product

Partnerships with Ecosystem Leaders

CHIP
(Core EDA)

CHIP
(Core EDA)

Package and
Board

System Integration

System design
IP/SoC verification
System-level IP protocols
Software applications
Software development

System analysis

Packaging and PCB design

PCB design
Package design
PCB and package analysis
Chip-to-chip protocol IP

Design and implementation
IP/SoC verification
On-chip protocol IP
Dataplane unit IP
Software drivers

Protium, Palladium
Hybrid, VSP

Innovus
Digital Design
Platform

Innovus
Digital Design
Platform

Virtuoso
Analog, Custom, RF,
Mixed-signal Design
Platform

Virtuoso
Analog, Custom, RF,
Mixed-signal Design
Platform

Cadence
Design IP
and Verification
IP

Cadence
Design IP
and Verification
IP

Allegro
Package and
PCB Design,
OrCAD PCB
Design

Allegro
Package and
PCB Design,
OrCAD PCB
Design

Incisive
Verification
Platform

Incisive
Verification
Platform

Mobile
Consumer
Cloud
Datacenter
Automotive
Medical
IoT
Cadence Tensilica Processor IP
For automotive applications

Digital radio and voice command
- Multi-microphone voice command, and noise reduction
- Multi-channel audio decode and advanced post processing
- Acoustic noise cancellation
- Digital Radio receiver: HD Radio, DAB, DAB+, DRM, T-DMB

Embedded signal processing
- Battery management
- Regenerative power management
- Engine control
- Cabin environmental control

ADAS vision processing
- Advanced Driver Assistance Systems
- Traffic sign detection / recognition
- Lane-departure warning
- Front-collision warning
- Automatic high beam

Telematics connectivity
- Emergency Services
- GPS
- Peer-to-peer smart car networking for intelligent vehicle highway control
- Built-in LTE Modem and WiFi Access Point
Cadence Design IP
For automotive applications

Memory Controllers and PHYs
- DRAM: DDR4, LPDDR4, DDR3, LPDDR3
- STORAGE: ONFI 4, ONFI 1/2/3, Toggle 1/2, UFS 2.0, SD/SDIO, eMMC, SATA PHY Gen 1, 2, 3, 3.1
- DDR/LPDDR3/4 Combo PHY
- DDR1/2, LPDDR1/2

Interfaces Controllers and PHYs
- DISPLAY: HDCP 2.2, HDMI 2.0 MHL 3.x, DP 1.3/eDP 1.4
- MIPI: SoundWire/SLIMbus, CSI-2/DSI, UniPro 1.6, DigRF v4, D-PHY 1.1
- ETHERNET: AVB/TSN MAC, 1000Base-T1 PHY, SGMII/QSGMII PHY
- USB: USB 1/2/3 Host, USB 1/2/3 Device, USB 1/2/3 OTG, USB 1/2/3 PHY with Type-C
- PCIe®: Controller for PCIe 1/2/3.0, PHY for PCIe 1/2/3.0

Analog
- ANALOG MIXED SIGNAL:
  - 6Gbps Multi-Protocol SerDes
  - 3.2GHz 7-bit ADC/DAC
  - 320MHz 12-bit ADC
  - VT Monitors
  - PLL/DLL

A broad and growing solution for your next SoC
Cadence Automotive IP

Processor, Design and Verification IP
- Advanced Driver Assistance Systems (ADAS)
- Wired and wireless connectivity
- Infotainment
- Electronic Control Units (ECU)

Processor IP
- Vision, Audio, Radar / Lidar
- ISO 26262 / ASIL ready to support your qualification efforts

Design IP
- Interfaces, Memory, Peripherals, Analog Mixed Signal
- AEC-Q100 support for your certification efforts

Verification IP portfolios
- Provides standard interfaces support for automotive IP, regardless of supplier
Cadence System Development Suite
Virtual or FPGA prototyping, simulation acceleration, and system emulation

Virtual Prototyping
Virtual System Platform
- Tensilica® SystemC models
- TLM 2.0 SystemC modeling
- Cycle accurate or fast functional at the transaction or pin level
- Early driver/firmware development
- Rich component model library
- Connection to hardware engines for hybrid co-execution

IP Sub-system Prototyping
RIPE2 IP Eval Board
- Low cost
- Single protocol validation
- Small sub-system demo
- Multi-slot HPC FMC for pluggable PHY-daughter cards
- Software/firmware drivers for interface IP

FPGA Prototyping
Protium™ Platform
- Early software development for sub-system in context of system environment
- FPGA prototyping environment compatible to Palladium® flow, allowing sub-system extension
- Multi-FPGA partitioning, clock management, memory mapping, SpeedBridge® support
- System validation

HW-SW Co-Verification
Palladium Platform
- Comprehensive verification computing platform from node to hub to cloud
- Scalability and flexibility up to 2.3 billion gates and 512 users
- Simulation acceleration
- Flexible resource allocation
- SpeedBridge adapter to high-speed interface to allow interface with real-world environment

Reduced Time to Market with Comprehensive Solutions
Collaboration between Cadence & Dassault on Traceability

- First "file-based" integration of Reqtify into vManager already exists
- At next step direct integration based on vManager Tool API planned
- Discussions about further integrations

- Presented by Michael Seibt, Dassault, at CDNLive Munich 2015
Case study: HEVC / H.265
HLS helps Renesas to be first to market

• Challenges:
  – Develop H.265-compliant IP with proprietary new algorithm in time to lead the market
  – Support multiple PPA and I/O requirements of mobile, consumer, vehicle information systems, industrial equipment

• Results:
  – 70% reduction in design and verification time
  – 6x faster verification
  – Utilized HLS ECO Flow to overcome late functional change
  – Planned for implementation in the third generation of the Renesas R-Car series of system on a chip (SoC) products for vehicle information systems

“Deploying the system-level design approach … for the entire design addressed this challenge, and we were able to implement the new algorithm very efficiently, achieving a good time-to-market for our advanced new IP.”

Toyokazu Hori – Department Manager, Renesas Electronics Corporation
Cadence functional safety verification
New solution within the Cadence System Development Suite

- Reduces effort by up to 50%
  - Eliminates testbench refactoring
  - Automates fault simulation execution

- Safety requirements tracing
  - Integrated regression throughout for compliance metrics
  - Integrated permanent and transient fault simulation

- Higher performance/capacity
  - Gate-level, Verilog, and VHDL
  - Digital / mixed-signal simulation
  - Verify with IEEE languages
Connecting Functional Verification, Formal Verification, and Safety Analysis in vManager

- Paper by Michael Rohleder, Freescale – 29 April 2015
- Value: automate connection of requirements to formal and simulation results
QCOM (CSR) Automotive Infotainment early Software bring-up using the Palladium platform

- ARM-based infotainment SoCs
- System & early firmware validation
- 200x speed-up for OS bring-up with Palladium® Hybrid technology
- CSR shaved months off schedule

“For our market-leading infotainment system offerings, differentiation using software is key, and pre-silicon OS bring-up becomes an important tapeout condition. Using the Cadence Palladium Hybrid technology, we saw orders of magnitude speed-up for early Linux and Android bring-up, allowing efficient pre-silicon software development and testing for our ARM-based SoC.”

– Nir Maor, Senior Director, Architecture and Digital Design, CSR plc
Innovus for layout safety requirements

• Redundancy via Triple Voting Flops (TVF)
  – 3 registers drive a majority value decision making cell
  – TVF set cannot share the same physical well

• Safety islands
  – Main and checker cores run same program
  – One clock cycle delay enables comparison every clock cycle
  – Totally independent cells and routing
  – Ensures safety island logic contained within a physical region
Auto IC Reliability
Design
Around
Transistor
Degradation

1. Fresh test (time is zero)
2. Stress test (generate degradation data)
   - Extreme environmental conditions are used to stress devices
   - Hot Carrier Injection, Positive/Negative Bias Temperature Instability
3. Aged test (eg 1, 3 or 10 yrs)
Auto IC Reliability
Design Around Interconnect Degradation

- Capacitance Computed
- Resistance Computed
- Electromigration Current Violation

Layout-Aware Re-simulation

Cadence® Virtuoso® Electrically Aware Design
Auto IC Reliability
Design Around Manufacturing Variation

Multi-Test Environment
Sweeps, Corners, Monte Carlo across tests
Worse Case Corners

Spec-driven design environment for easy verification of design performance
Parameterize designs without editing schematics

Compare simulation history

Explore the vast design space & electrical sign-off in hours not days or weeks
Auto IC Reliability
Design Around Manufacturing Variation
Sub-20nm Increased Variation

- Complexity of effects cannot be easily anticipated
- Mitigation creates over-design or long iteration loops

- Layout-Dependent Effects change transistors characteristics
  - Typically by 20% & up to 80%
  - $I_{dsat}$, $V_{th}$, mobility, body effect, drain induced barrier lowering, $g_m$, ...

<table>
<thead>
<tr>
<th>Layout Dependent Effects</th>
<th>Prior to 40nm</th>
<th>At 40nm</th>
<th>20nm &amp; Below</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPE</td>
<td>x</td>
<td>x</td>
<td>x</td>
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<tr>
<td>Well Proximity Effect</td>
<td></td>
<td></td>
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<tr>
<td>PSE</td>
<td>x</td>
<td></td>
<td>x</td>
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<tr>
<td>Poly Spacing Effect</td>
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</tr>
<tr>
<td>LOD</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Length of Diffusion</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>OSE</td>
<td>x</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>OD to OD Spacing Effect</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Layout Dependent Effects
- WPE: Well Proximity Effect
- PSE: Poly Spacing Effect
- LOD: Length of Diffusion
- OSE: OD to OD Spacing Effect

Device under consideration

WPE LDE Introduces mismatch between M1 and M2

Well Proximity Effect

Poly Spacing Effect

Length of Diffusion

OD to OD Spacing Effect

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Auto PCB/Package/IC Reliability
Design Around Electromagnetic Interference and Thermal

Cadence® Sigrity® PowerDC™
Cadence® Sigrity® PowerSI® 3D-EM
“Cadence Sigrity technology dramatically reduced EMI/EMC testing time. And our product went to market was much faster.”

Imran Shak – Hyundai MOBIS
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• Call to action
Call to Action

- Seek rigorous design and verification
  - Functional quality is a business advantage

- Implement safety verification
  - Automated process can save millions per year

- Look to the future
  - Safety and dependable design will be pervasive
  - Skills developed for automotive will go beyond safety critical markets
  - Industry collaboration on automation and higher abstraction
Cadence Provides ADASoC Automation

- Enhance core technology – quality, performance, integration
- Innovate technology and methodology – application focused
- Connect design chain – technology, standards, collaboration